Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the Application:

Listing of Claims:

1. (currently amended) A thin film transistor array panel, comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode;

a first protrusion formed directly on at least a portion of the first passivation layer and disposed opposite the data line;

and,

a pixel electrode formed directly on the first passivation layer and connected to the drain electrode.

2. (original) The thin film transistor array panel of claim 1, wherein the pixel electrode has a cutout.

3. (original) The thin film transistor array panel of claim 2, further comprising a second protrusion disposed in the cutout.

4. (original) The thin film transistor array panel of claim 2, further comprising a storage electrode line overlapping the pixel electrode.

5. (original) The thin film transistor array panel of claim 4, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

6. (original) The thin film transistor array panel of claim 4, wherein the storage elec-

trode line comprises a branch overlapping the cutout.

7. (withdrawn) The thin film transistor array panel of claim 1, wherein the first protrusion is wider than the data line.

8. (withdrawn) The thin film transistor array panel of claim 1, wherein the data line is curved.

9. (withdrawn) The thin film transistor array panel of claim 1, further comprising a spacer having a height larger than the first protrusion and disposed on the same layer as the first protrusion.

10. (withdrawn) The thin film transistor array panel of claim 9, wherein the first protrusion and the spacer comprise organic material.

11. (withdrawn) The thin film transistor array panel of claim 1, further comprising a color filter disposed between the first passivation layer and the first protrusion and the pixel.

12. (withdrawn) The thin film transistor array panel of claim 11, further comprising a second passivation layer formed on the color filter and the first protrusion and the pixel electrode.

13. (withdrawn) The thin film transistor array panel of claim 1, wherein the semiconductor layer has substantially the same planar shape as the data line and the drain electrode.

14. (currently amended) A thin film transistor array panel, comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode and having a con-

tact hole exposing the drain electrode at least in part;

a pixel electrode formed directly on the first passivation layer and connected to the drain electrode through the contact hole, the pixel electrode having a cutout; and,

a protrusion formed directly on at least a portion of the first passivation layer and disposed in the cutout at least in part.

15. (original) The thin film transistor array panel of claim 14, further comprising a storage electrode line overlapping the pixel electrode.

16. (original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

17. (original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises a branch overlapping the cutout.

18. (withdrawn) The thin film transistor array panel of claim 14, wherein the data line is curved.

19. (original) The thin film transistor array panel of claim 14, further comprising a spacer having a height larger than the protrusion and disposed on the same layer as the protrusion.

20. (original) The thin film transistor array panel of claim 19, wherein the protrusion and the spacer comprise organic material.

21. (previously presented) The thin film transistor array panel of claim 14, comprising a color filter disposed between the first passivation layer, and the protrusion and the pixel electrode.

22. (previously presented) The thin film transistor array panel of claim 21, further comprising a second passivation layer formed on the color filter and intermediate to the protrusion and the pixel electrode.

23. (currently amended) The thin film transistor array panel of claim 14 [[1]], wherein

the semiconductor layer has substantially the same planar shape as the data line and the drain electrode.

24. (withdrawn) A liquid crystal display comprising:

a first substrate;

a gate line formed on the first substrate;

a data line intersecting the gate line;

a thin film transistor connected to the gate line and the data line;

a pixel electrode connected to the thin film transistor and having a first cutout;

a second substrate facing the first substrate;

a common electrode formed on the second substrate and having a second cutout; and,

a first protrusion disposed in at least one of the first and the second cutouts at least in part.

25. (withdrawn) The liquid crystal display of claim 24, further comprising:

a light blocking member disposed on one of the first and the second substrates; and,

a color filter disposed on one of the first and the second substrates.

26. (withdrawn) The liquid crystal display of claim 24, further comprising a second protrusion disposed on the data line.

27. (withdrawn) The liquid crystal display of claim 24, wherein the first cutout does not overlap the second cutout.